WHAT IS CLAIMED IS:

1. A method for down-loading data from an upper processor to a plurality of lower processors of a mobile communications switching system in a process of resetting the processors, the method comprising:

requesting an information down-load from the lower processors to the upper processor;

accessing a memory of the upper processor containing the requested information down-load;

determining whether the accessed information has an error;

grouping the lower processors with a representative address; and

creating the accessed information in an IPC format and transferring the IPC format information by using the group representative address.

2. The method of claim 1, wherein the resetting of the processors includes an initial loading and a re-loading.

3. The method of claim 1, wherein the group representative address includes all the lower processors.

4. The method of claim 1, wherein the grouping the lower processors comprises grouping the plurality of lower processors using the group representative address.

5. The method of claim 1, wherein the grouping the lower processors comprises grouping at least one additional lower processor.

6. The method of claim 1, wherein group information is used to determine the group representative address, and wherein the group information comprises a node address (NA), a BHIU address (BA), a cinu address (CA), and a slot address (SA).

7. The method of claim 6, wherein the group representative address is set by using the CA and the SA among the group information.

8. The method of claim 7, wherein grouping of the group representative address is responsive to one of only the CA among the group information, only the SA among the group information and both the CA and the SA among the group information.

9. The method of claim 8, wherein the IPC format information is concurrently transferred to all the lower processors using the group representative address.

10. A method for down-loading data from a first processor to a plurality of second processors while resetting the processors, the method comprising:

transmitting a request for an information down-load from the plurality of second processors to the first processor;

accessing once a memory of the first processor for the requested information;

grouping the second processors using a prescribed processor address; and

assembling the accessed information in a prescribed format and transferring the assembled requested information to at least two second processors using a group representative address.

11. The method of claim 10, wherein the grouping of the plurality of lower processors is performed using the group representative address.

12. The method of claim 10, wherein the prescribed processor address is an IPC processor address that includes a node address (NA), a BHIU address (BA), a cinu address (CA), and a slot address (SA).

13. The method of claim 12, wherein the group representative address is set by using the CA and the SA among the IPC processor address.

14. The method of claim 13, wherein grouping of the group representative address is responsive to one of the CA, the SA and both the CA and the SA.

15. The method of claim 10, wherein the method further comprises determining whether the accessed requested information has an error.